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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/788,560	01/24/97	YAMAZAKI S	0756-1626

MMC1/0728
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EXAMINER	
NADAV.O	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/28/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/788,560	Applicant(s) Yamazaki et al.
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Jan 16, 1900* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *78-157* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *78-157* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Jan 24, 1997* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *31*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a pixel electrode connected to a semiconductor film in a device comprising a gate electrode under the channel region with gate insulating film interposed therebetween, as recited in claims 146 and 152 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 78-93, 95-99, 101-103, 105-107, 109-111, 113-115, 117-119, 121-127 and 129-133 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. (4,755,865) in view of Saito et al. (4,772,927) and Shizukuishi et al. (4,841,348). Wilson et al. teaches in figure 3 substantially the entire claimed structure, including a MOS transistor comprising a semiconductor film 42 comprising a channel region 42B in between source and drain regions 42A, a gate electrode 44 adjacent the channel region with gate insulating film 43 interposed therebetween, wherein each of the source and drain regions has a portion 42C containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E15 atoms per cm cube or more (column 4, lines 39-49), wherein the channel region containing boron (column 6, lines 31-32).

Wilson et al. do not teach a MOS transistor being used in a CMOS device, which is part of a peripheral circuit of an active matrix type device having plurality of pixels. However, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). In this case, using a MOS transistor in a CMOS device, and using the CMOS device in a peripheral circuit of an active matrix type device having plurality of

pixels is a recitation of the intended use of a structure which does not add to the structural limitations in the body of the claim

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Therefore, the claimed structure is considered to be in at least obvious over the Wilson et al.'s structure.

In the alternative, Saito et al. teach a MOS transistor in figure 1e comprising a semiconductor film comprising crystalline silicon (column 1, lines 19-20) and a channel region 7 in between source and drain regions 6, a gate electrode 9 adjacent the channel region with gate insulating film 5 interposed therebetween, wherein the source and drain regions have at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E19 atoms per cm cube or more (column 3, line 49 to column 4, line 24), formed in a CMOS device (figure 2).

Shizukuishi et al. teach a MOS transistor being used in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels

(abstract), and formed of a semiconductor film comprising amorphous silicon (column 3, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Wilson et al.'s transistor in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels, because it is conventional in the art to connect individual transistors in order to form a CMOS device, and it is well known in the art to use CMOS transistors in a peripheral circuit of an active matrix type device having plurality of pixels. The combination is motivated by the teachings of Saito et al. who point out the advantages of using a TFT transistor having source and drain regions containing carbon, nitrogen or oxygen at a concentration higher than 10E19 atoms per cm cube or more in a CMOS device.

Regarding claims 90, 96, 105, 111, 119 and 127 although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s

device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 102, 110, 118 and 126, Saito et al. teach a channel region having at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E19 atoms per cm cube or more (column 5, lines 20-23).

5. Claims 94, 100, 108 and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al. and Shizukuishi et al., as applied above, and further in view of Solheim (5,219,784).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, as above, except a threshold voltage of an NMOS being approximately equivalent to that of the PMOS.

Solheim teaches a threshold voltage of an NMOS being approximately equivalent to that of the PMOS (column 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use of a threshold voltage of an NMOS being approximately equivalent to that of the PMOS in Wilson et al.'s device, since adjusting the threshold

voltage is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization, depending on the intended use of the device.

6. Claims 104, 112, 120 and 128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. and Saito et al., as applied to claims 102, 110, 118, 126 above, and further in view of Higashi et al. (4,694,317).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, including a first interlayer insulating film (ILD) 10 (Saito et al.) comprising inorganic material, and a gate electrode comprising a silicon film containing phosphorus (Wilson et al., column 3, lines 38-40, and column 6, line 32). Wilson et al. and Saito et al. do not teach a second ILD film comprising organic resin and a pixel electrode on the second ILD film formed in a transparent or a reflective device.

Higashi et al. teach in figure 1D a transparent or a reflective device comprising a first interlayer insulating film 5 comprising inorganic material, a second ILD film 7 comprising organic resin and a pixel electrode 11 on the second ILD film (column 3, line 64 to column 4, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second ILD film comprising organic resin under a pixel electrode in Wilson et al.'s device, in order to provide better protection for the device.

The combination is motivated by the teachings of Higashi et al. who point out the advantages of using an organic ILD film under a pixel electrode in a TFT transistor.

7. Claims 134-157 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. or Saito et al. in view of Parks et al. (4,646,424).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, as applied above, except a pixel electrode connected to the semiconductor film.

Parks et al. teach in figure 4J a pixel electrode 16 connected to the semiconductor film 24b. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the pixel electrode to the semiconductor film in Wilson et al. and Saito et al.'s device, in order to be able to operate the device.

Regarding claims 134, 140, 147 and 153, although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s

device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 146 and 152 Parks et al. teach a gate electrode under the channel region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the gate electrode under the channel region in Wilson et al. and Saito et al.'s device, because it is conventional in the art to form the gate in thin film transistor either over or under the channel region. Note Schachter et al. is cited to support the well known position.

Response to Arguments

8. Applicant argues on pages 21-22 that it is advantageous to use the invention in a peripheral circuit of a display device. However, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

Ori Nadav, Ph.D.

July 27, 2000